1. A method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate, comprising the steps of:

providing a semiconductor substrate of a first conductivity type;

forming a silicon on insulator (SOI) layer on said semiconductor substrate;

forming an insulator filled, shallow trench isolation (STI) region in the silicon component of the SOI layer, with depth of said STI terminating at the top surface of the insulator component of said SOI layer;

forming a gate insulator layer on surface of said silicon component of said SOI layer;

forming a conductive gate structure on said gate insulator layer, and on a portion of said STI region;

forming a body contact region in a first portion of said silicon component of said SOI region; and

forming a source/drain region in a second portion of said silicon component of said SOI layer, wherein said second portion of said silicon component of said SOI layer is separated from said first portion of said silicon component of said SOI layer by said STI region.

2. The method of claim 1, wherein said semiconductor substrate of said first conductivity type, is a P type semiconductor substrate.

3. The method of claim 1, wherein said insulator component of said SOI layer is a silicon oxide layer formed at a thickness between about 1000 to 3000 Angstroms.

4. The method of claim 1, wherein said silicon component of said SOI layer is formed at a thickness between about 1000 to 3000 Angstroms.

5. The method of claim 1, wherein said STI region is formed with an area between about 2Lg x 2Lg to 10Lg x 10Lg um^2, wherein Lg is the gate length.

6. The method of claim 1, wherein depth of said STI region is between about 1000 to 3000 Angstroms.

7. The method of claim 1, wherein said STI region is filled with silicon oxide.

8. The method of claim 1, wherein said gate insulator layer is a silicon dioxide layer, thermally grown to a thickness between about 10 to 100 Angstroms.

9. The method of claim 1, wherein said conductive gate structure is comprised of polysilicon, at a thickness between about 1000 to 2000 Angstroms.

10. The method of claim 1, wherein an NMOS device is comprised with a N type source/drain region obtained via implantation of arsenic or phosphorous ions at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 $atoms/cm^2$.

11. The method of claim 1, wherein a PMOS device is comprised with a P type source/drain region, obtained via implantation of boron or BF_2, at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2, and comprised with an N type body contact region obtained via implantation of arsenic or phosphorous, at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2.

12. A method of forming a MOSFET device on a silicon on insulator (SOI) layer, featuring insulator filled, shallow trench isolation (STI) regions used to reduce parasitic transistor formation underlying the junction of conductive gate structure and a body contact region, comprising the steps of:

forming said SOI layer on a P type semiconductor substrate, with said SOI layer comprised of an underlying silicon oxide layer, and an overlying silicon layer;

forming shallow trench shapes in said silicon layer exposing top surface of said insulator layer;

filling said shallow trench shapes with silicon oxide resulting in insulator filled, STI regions in said silicon layer.

forming a silicon dioxide gate insulator layer on said silicon layer;

forming a polysilicon gate structure on said silicon dioxide gate insulator layer and on portions of said STI regions, with shape of said polysilicon gate structures separating an active device region on a first portion of said silicon layer, from non-active device regions located on second portions of said silicon layer;

defining a P type or N type body contact region in said second portion of said silicon layer; and

forming N type or P type source/drain region in an area of said first portion of said silicon layer not covered by said polysilicon gate structure.

not covered by said polysilicon gate structure for a P channel device.

13. The method of claim 12, wherein said silicon oxide layer of said SOI layer is formed at a thickness between about 1000 to 3000 Angstroms.

14. The method of claim 12, wherein said silicon layer of said SOI layer is formed at a thickness between about 1000 to 3000 Angstroms.

15. The method of claim 12, wherein said shallow trench shapes are formed via reactive ion etching procedures to a depth between about 1000 to 3000 Angstroms.

16. The method of claim 12, wherein said STI regions are formed with an area between about 2Lg x 2Lg to 10Lg x 10Lg um^2, wherein Lg is the gate length.

17. The method of claim 12, wherein said silicon dioxide gate insulator layer is thermally grown to a thickness between about 10 to 100 Angstroms.

18. The method of claim 12, wherein the thickness of said polysilicon gate structure is between about 1000 to 2000 Angstroms.

19. The method of claim 12, wherein said polysilicon gate structure is defined as a "T" shape gate structure..

20. The method of claim 12, wherein said polysilicon gate structure is defined as an "H" shape gate structure.

21. The method of claim 12, wherein P type source/drain region is formed in said first portions of said silicon layer via implantation of boron or BF_2 ions at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2.

22. The method of claim 12, wherein N type source/drain region is formed in said first portion of said silicon layer via implantation of arsenic or phosphorous ions at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2.

23. A MOSFET device structure, comprising:

an insulator layer on a semiconductor substrate;

a silicon shape on said insulator layer;

an insulator filled, shallow trench isolation (STI) region in said silicon shape, with said STI region terminating at the top surface of said insulator layer;

a gate insulator layer on portions of the top surface of said silicon shape not occupied by said STI region;

a "T" shaped conductive gate structure comprised with a horizontal component on said gate insulator layer located on a first portion of said silicon shape and comprised with a vertical component attached to said horizontal component of said conductive gate structure, with the junction of said vertical portion of said conductive gate structure and said horizontal portion of said conductive gate structure overlying a portion of said STI region, and with said vertical portion of said conductive gate structure and said STI region separating said first portion of said silicon shape from a second portion of said silicon shape;

a body contact region in said second portion of said silicon shape; and

a source/drain region in an area of said first portion of said silicon shape not covered by said horizontal component of said conductive gate structure.

24. The MOSFET device structure of claim 23, wherein said semiconductor substrate is a P type semiconductor substrate;

25. The MOSFET device structure of claim 23, wherein said insulator layer is a silicon oxide layer, at a thickness between about 1000 to 3000 Angstroms.

26. The MOSFET device structure of claim 23, wherein the thickness of said silicon shape is between about 1000 to 3000 Angstroms.

27. The MOSFET device structure of claim 23, wherein said STI region is filled with silicon oxide.

28. The MOSFET device structure of claim 23, wherein the depth of said STI region is between about 1000 to 3000 Angstroms.

29. The MOSFET device structure of claim 23, wherein the area of said STI region is between about 2Lg x 2Lg to 10Lg x 10Lg um^2, wherein Lg is the gate length.

30. The MOSFET device structure of claim 23, wherein the width of said conductive gate structure is between about 10 to 350 um.

31. The MOSFET device structure of claim 23, wherein said conductive gate structure is comprised of polysilicon at a thickness between about 1000 to 2000 Angstroms.

32. The MOSFET device structure of claim 23, wherein said body contact region is a P type or N type body contact region.

33. The MOSFET device structure of claim 23, wherein said source/drain region is an N type or P type source/drain region.

34. A MOSFET device structure, comprising:

an insulator layer on a semiconductor substrate;

a silicon shape on said insulator layer;

insulator filled, shallow trench isolation (STI) regions in said silicon shape, with each STI region terminating at the top surface of said insulator layer, and with space between said STI regions defining a first portion of said silicon shape;

a gate insulator layer on portions of the top surface of said silicon shape not occupied by said STI regions;

an "H" shaped conductive gate structure comprised with a horizontal component on said gate insulator layer located on said first portion of said silicon shape, and comprised with verticals component each attached to each end of said horizontal component of said conductive gate structure, with the junctions of the vertical portions of said conductive gate and the horizontal portion of said conductive gate structure overlying a portion of an STI region, and with combination of each vertical portion of said conductive gate structure and STI region separating said first portion of said silicon shape from second portions of said silicon shape;

a body contact region in said second portions of said silicon shape; and

a source/drain region in an area of said first portion of said silicon shape not covered by said horizontal component of said conductive gate structure.

35. The MOSFET device structure of claim 34, wherein said semiconductor substrate is a P type semiconductor substrate;

36. The MOSFET device structure of claim 34, wherein said insulator layer is a silicon oxide layer, at a thickness between about 1000 to 3000 Angstroms.

37. The MOSFET device structure of claim 34, wherein the thickness of said silicon shape is between about 1000 to 3000 Angstroms.

38. The MOSFET device structure of claim 34, wherein said STI regions are filled with silicon oxide.

39. The MOSFET device structure of claim 34, wherein the depth of said STI regions is between about 1000 to 3000 Angstroms.

40. The MOSFET device structure of claim 34, wherein the area of said STI regions is between about 2Lg x 2Lg to 10Lg x 10Lg um^2, wherein Lg is the gate length.

41. The MOSFET device structure of claim 34, wherein the width of said conductive gate structure is between about 10 to 350 um.

42. The MOSFET device structure of claim 34, wherein said conductive gate structure is comprised of polysilicon, at a thickness between about 1000 to 2000 Angstroms.

43. The MOSFET device structure of claim 34, wherein said body contact region is a P type or N type body contact region.

44. The MOSFET device structure of claim 34, wherein said source/drain region is an N type or a P type source/drain region.